# SIGNAL DETECTOR

## RELATED U.S. APPLICATIONS

Not applicable.

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not applicable.

## REFERENCE TO MICROFICHE APPENDIX

Not applicable.

## FIELD OF THE INVENTION

**[0001]** This invention serves as a signal detector. It is specifically designed to instantly detect and react by outputting a driver signal to alert the user of the problem when interruptions or abnormality in clock and data signal transmission occurs. This device utilizes a clock signal detector to monitor the status of clock signal. When clock signal is interrupted, the signal converter and rectifying-filtering circuit cease to output corresponding signal and D.C. potential signal. Once this is detected, the inverter then outputs a high-potential signal to warn the user of the detected abnormality in clock signal. Another major component of this invention is the Data Signal Detector. It is designed to detect abnormality in data signal transmission. When the data ratio of the positive potential signal in the data signal transmission becomes overly high, the signal converter and integral charger output a corresponding high ratio data signal and integral potential signal. Once the output surpassed the standard level of potential, the inverter is then driven to output a low-potential signal as an alert to

the user for the abnormality in data signal transmission. With this mechanism, the data transmission signal detector is able to instantly detect abnormal transmission and react by outputting a potential signal to alert the user, and, in turn, protect the data transmission facility as well as reducing time and resource wastages.

## BACKGROUND OF THE INVENTION

**[0002]** There are numerous types of detectors in the market for various uses, such as fire warning, anti-theft, quantity surveying, etc. Basically, these detection devices utilize temperature, pressure, or light sensors to detect variations in temperature, air pressure, and light, and then send out signals for warning.

**[0003]** However, currently, very few commonly seen transmission facilities are equipped with signal detection functions. Therefore, once the clock signal is interrupted during a transmission, the whole course of transmission is interrupted as well without any warning. Such interruptions often cause delays in time as well as transmission, and in turn cause wastages in valuable resources. Also, during data transmission, if a short circuit or other factors cause the system to continuously output a series of data signals, the abnormal data transmission may cause the transmission facility as well as the laser to become overly exhausted or even break down.

## BRIEF SUMMARY OF THE INVENTION

**[0004]** Improvements to previous technologies and new effects expected from this invention:

**[0005]** 1. This signal detector is equipped with a clock signal detector 10, which is connected to the clock signal path in the data transmission. When clock signal-of the transmission is interrupted, the detector outputs a clock signal abnormality detection potential signal. This mechanism can effectively

prevent undetected interruptions during a clock signal transmission through fiber optics or other types of wires, and in turn prevent time and resource wastages.

**[0006]** 2. This signal detector is also equipped with a data signal detector 20, which is connected to the path of data signal in data transmission. When the data ratio of potential signal 1 from the data signal becomes overly high, the system outputs a data signal transmission abnormality detection potential signal. This mechanism can effectively prevent continuous emission of data signal during a short circuit or other system failures.

**[0007]** 3. The main functions of the clock signal detector 10 and the data signal detector 20 are designed to instantly detect interruptions in the clock signal transmission or abnormal transmission in data signals. Coordinated with an interruption control circuit, the system is able to prevent continuous laser emission and in turn prevent the laser emitter from sever exhaustion or breakdown.

**[0008]** 4. The clock signal detector 10, composed of a signal converter 11, a rectifying-filtering circuit 12, and an inverter 13, is capable of converting the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal into a Low-Voltage Transistor-Transistor Logic (LVTTL) signal, which is then coordinated with a D.C. potential signal outputted from the rectifying-filtering circuit and drives the inverter 13 to make an indicator for the clock signal, that is, output a clock signal transmission abnormality detection potential signal while clock input signal interrupts.

**[0009]** 5. The data signal detector 20, composed of a signal converter 21, integral charger 22, and an inverter 23, is capable of converting the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal into a Low-Voltage Transistor-Transistor Logic (LVTTL) signal, which is then inputted into a integrator and then outputted to the inverter 23 for reactions against the overly high data ratio output of potential signal 1 in the signal transmission, that is, output a data signal transmission abnormality detection potential signal while inputted data signal is pulled high abnormally.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

**[0010]** FIG. 1 shows the external wiring of the invention.

**[0011]** FIG. 2 shows the internal wiring of the invention.

**[0012]** FIG. 3 shows the internal wiring of the clock signal detector - an implemented example.

**[0013]** FIG. 4 shows the signal conversion procedures of the clock signal detector - an implemented example.

**[0014]** FIG. 5 shows the internal wiring of the data signal detector - an implemented example.

**[0015]** FIG. 6 shows the signal conversion procedures of the data signal detector - an implemented example.

**[0016]** FIG. 7 shows the internal wiring of the integral charger in the data signal detector - an implemented example.

**[0017]** FIG. 8 shows the integral signal detection procedures in the integral charger of the data signal detector- an implemented example.

## DETAILED DESCRIPTION OF THE INVENTION

**[0018]** a. Technical Problems Intended to Solve

**[0019]** This invention is designed to instantly detect interruptions in clock signal and abnormality in data signal transmission. When the interruption or abnormality is detected, the device reacts by outputting a driver signal to alert the user. This device is effective in shortening the delays in transmission and in turn raises the efficiency in time and resource utilization.

**[0020]** b. Technical Means Used to Solve the Problem

**[0021]** This invention aims to provide a type of signal detector that detects abnormality in clock and data signal transmission. The clock signal detector utilizes a signal converter, a rectifying-filtering circuit, and an inverter to instantly detect abnormal transmission in clock signal and react by

outputting a potential signal to alert the user of the detected abnormality. The clock signal detector functions when an interruption in the clock signal transmission occurs. When such situation occurs, the signal converter and rectifying-filtering circuit cease to output corresponding clock signal and D.C. potential signal. Once the interruption is detected, the inverter then outputs a high-potential signal to alert the user of the detected abnormality or to drive a interruption control circuit to cut off the power of the transmitter.

**[0022]** Furthermore, another major component in this invention is the data signal detector. It utilizes a signal converter, an integral charger, and an inverter to instantly detect abnormal transmission and outputs a potential signal as a warning. It functions when the input data ratio of the positive potential signal in data signal transmission becomes overly high. When this occurs, the signal converter correspondingly output a higher ratio data signal and then outputs the data signal to an integral charger to produce a higher integral potential signal. Once the output surpasses the defined potential level, the inverter then outputs a signal to alert the user of the detected abnormality in data signal transmission or to drive a interruption control circuit to cut off the power of the transmitter.

**[0023]** The features and the advantages of the present invention will be more readily understood upon a thoughtful deliberation of the following detailed description of the preferred embodiments of the present invention with reference to the accompanying drawings.

**[0024]** As shown in FIG. 1 and 2, the clock signal detector 10 can be connected to the path of clock signal transmission, and the data signal detector 20 can be connected to the path of data signal transmission. The clock signal detector 10 is design with the following components: (as shown in FIG. 2, 3, and 4)

**[0025]** A signal converter 11, which is the signal converter U1 between the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal input end and Low-Voltage Transistor-Transistor Logic (LVTTL) output end to convert coupled input differential clock signal into single input clock signal.

**[0026]**A rectifying-filtering circuit 12, which can be a stand-alone rectifying component (i.e. micro inductor L1) connected to the signal converter 11. It transforms the clock signal inputted from the signal converter into D.C. potential signal output.

**[0027]** An inverter 13, which is connected to the rectifying-filtering circuit 12 - It serves as a buffer for Inductor L1. At the input end, the regularly present D.C. potential signal is inputted into the base of Transistor Q3, the transistor Q3 will get into the status of "ON". Thus, the collector of the transistor Q3 regularly outputs a low potential signal. Conversely, when the clock signal disappears, in other words, no signal is inputted into the base of transistor Q3' and the transistor Q3 will get into the status of cut-off. Thus the collector of the transistor Q3 regularly outputs a high potential signal. Base on above description, this mechanism achieves the effect of inversion, and the signal outputted is the said clock signal transmission abnormality detection potential signal, which is the resulted potential signal output, reversed from the D.C. potential signal inputted from the rectifying-filtering circuit 12.

**[0028]** As shown in FIG. 4, the clock signal detector 10 functions when an interruption in clock signal transmission occurs. When the interruption occurs, the signal converter 11 and rectifying-filtering circuit 12 cease to correspondingly output clock signal and D.C. potential signal, which drives the inverter 13 to output a high-potential signal, that is, output a clock signal transmission abnormality detection potential signal.

**[0029]** Furthermore, as shown in FIG. 2, 5, and 6, the data signal detector 20 contains:

**[0030]** A signal converter 21, which acts as the Signal Converter U1 between the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal input end and the output end of a set of Low-Voltage Transistor-Transistor Logic (LVTTL) signal. This converter converts coupled input differential data signal into single output data signal.

**[0031]** An Integral Charger 22, which is connected to the signal converter 21, as shown in FIGS. 7 and 8. The second resister R2 of the integral charger is connected to the capacitor C2 in parallel, which is then connected to the first resister R1 with a tandem connection. In which, the first resistor R1 is the input end and the tandem connection point between the first resistor R1 and the second resistor R2 is the output end. The other end of the second resistor R2 is grounded, which also converts the data signal, inputted from the signal converter 21, into a pulse type integral potential signal and outputs it to the next stage. This potential signal approximately corresponds to a constant ratio of positive potential signal pulse.

**[0032]** An Inverter 23, which is connected to the integral charger 22; it serves as the Logic Gate U2 and makes logic decisions to the inputted integral potential signal. It decides the status of inverting by a internal threshold voltage which is setting in logic IC. If the data ratio of positive potential signal in the differential data signal is transmitted normally, in other words, the positive potential is less than the threshold voltage, then the inverter 23 will keep the original status. Conversely, when the data ratio of positive potential signal in the differential data signal transmission becomes overly high(higher than the threshold voltage), the inverter 23 will reverse the positive signal into a low-potential signal for output. But the above statement "the low-potential signal for output" is just an example, in fact, the high or low potential of signal must lies on the requirement of next stage. Through this mechanism, reversion is achieved, and the outputted signal is the so-called data signal transmission abnormality detection potential signal, which is the potential signal output reversed from the integral potential signal inputted from the integral charger 22.

**[0033]** In summary, the data signal detector 20, as shown in FIGS. 6 and 8, is capable of detecting overly high ratio of potential data signal output, when the data ratio of positive potential signal in the differential data signal transmission becomes overly high, the signal converter 21 and integral charger 22 correspondingly output a higher ratio data signal and integral potential signal, and when the output

surpassed the defined potential level, the inverter 23 outputs a low-potential signal, that is, the data signal transmission abnormality detection potential signal.

**[0034]** In which, the output end of the clock signal detector 10 and data signal detector 20, as shown in FIG. 1 and 2, are individually connected to the interruption control circuit (30) at the emission ends of the transmission system (i.e. laser emitter of the fiber-optic transmitter end). The data signal transmission abnormality detection potential signal, in conjunction with the clock signal abnormality detection potential signal, is used to drive the interruption control circuit to stop the signals from being continuously emitted.

**[0035]** This interruption control circuit 30 contains a Transistor Q1 circuit. When the clock signal transmission is at a normal status, the clock signal detector 10 outputs a regularly present low D.C. potential signal into the base of the transistor Q1, which maintains the transistor Q1 in a "cut-off" state. The collector of Transistor Q1 then sends out a high D.C. potential signal to the originator of FET Transistor Q2. At this time, due to the input of high D.C. potential signal, the FET Transistor Q2 stays in a "cut-off" state - not sending out any interruption signals; therefore, the interruption control circuit 30 takes no action. The interruption control circuit only acts when the data signal detector 20 inputs a low-potential signal of data signal transmission abnormality detection into the originator of FET Transistor Q2, or when the clock signal detector 10 inputs a high-potential signal of clock signal abnormality detection into the base of Transistor Q1 to initiate the circuit between the collector and emitter of Transistor Q1. The interruption control circuit only acts to cease the operation of the emitting end of the transmission system when the originator of FET Transistor Q2 is in a "ON" state.

**[0036]** As shown in FIGS. 7 and 8, the potential of the integral charger 22 in the Data signal detector 20 starts to integrate upwards from the initial potential (Vinitial). The slope of upward integration is determined by the R-C time constant TC in the integral charger 22 circuit. Normal data signal output

should not stay as positive potential pulse signal for a long period of time. The above-mentioned Vinitial is configured based on the assumption of a normal data transmission state. It is configured based on a voltage calculated from positive/negative spaced integration of a pulse - Va * VR/2; the threshold voltage of inverter 23 is Vt' the integral output potential is Vb and the charge formula is Vb = Va * VR * [1-e(-t/TC)] + Vinitial e raise the power of (-t/TC). In this invention:

TC = R1 * R2 * C2/(R1+R2)

VR = R2/(R1+R2)

Vinitial = Va * VR/2

**[0037]** This integral output potential Vb approximately corresponds to a data pulse which constantly stays as a positive potential. When the data ratio of potential signal in the data pulse becomes overly high, the integral potential rises correspondingly, and when the integral output potential Vb surpasses the threshold voltage Vt, an abnormality in data transmission is indicated. Once this occurs, the detector sends out a low-potential D.C. signal through this IC Logic Gate U2 (which is the equivalent of the inverter 23). This signal is the said data signal transmission abnormality detection potential signal. If data transmission is in a normal state, the detector outputs a high-potential D.C. signal, and the above-mentioned threshold voltage serves as the determinant potential to decide whether the inverter 23 should output a reverse signal; that is, the potential must be higher then this threshold voltage for the inverter to initiate a reaction.

**[0038]** The clock signal detector 10 sends out a clock detection signal to the base of Transistor Q1 in the interruption control circuit 30. If the clock signal is in a normal state, this detection signal is outputted as zero potential, which maintains Transistor Q1 in an "OFF" state, and, based on the behavior of the Transistor Q2 in the interruption control circuit 30, the detector does not output a ShutDown signal to the driver device. Conversely, if the clock signal ceases to be present, Transistor

Q1 is then turned to the "ON" state and outputs a ShutDown signal to the control driver device, which will then stop the signal emission.

**[0039]** The Data signal detector 20 outputs data detection signals to the gate of Transistor Q2 in the interruption control circuit 30. When data signal transmission is in a normal state, the detection signal is outputted in high potential; therefore, the control circuit 30 does not output a ShutDown signal to the driver device. Conversely, if abnormal data signal transmission occurs, the interruption control circuit 30 outputs a ShutDown signal to the emission end of the transmission system, which will then stop the signal emission.